REMARKS

This paper responds to the Office Action mailed on February 12, 2007.

Claims 11 and 15 are amended, claims 18-25, 35-39 and 41-43 are canceled; as a result, claims 11-17 are now pending in this application.

Applicant informs the Examiner of the publication of patent family member 2006/0261445 on November 23, 2006.

§103 Rejection of the Claims

Claims 11-25, 35-39 and 41-43 were rejected under 35 U.S.C. § 103(a) as being unpatentable over "INTEGRATED CIRCUITS – Design Principles and Fabrication" (1965 textbook) taken with DEVICE ELECTRONICS for INTEGRATED CIRCUITS (1986 textbook), in view of Yamada (U.S. 5,266,528) and Chittipeddi et al. (U.S. 5,751,065), along with Altavela, et al. (U.S. 5,408,739). Applicant respectfully traverses this rejection, and notes that claims 18-25, 35-39 and 41-43 are canceled herein.

The cited '65 reference is used to disclose sawn die that have active areas and inactive areas. The Examiner states on page 3 of the outstanding Office Action that the rough edges shown have seen "improvements in separation" that "led to smoother perimeter side surfaces as seen for the 1970 chip in Fig. 2.1" (assumed by Applicant to be referring to the '86 text discussed below). Nevertheless, Applicant again submits that there is nothing in the reference to suggest bringing the edge of the scribe lane close to the edge of the active area. The section previously indicated by the Examiner (summary point 8 on page 162) actually teaches away from bringing the scribe edge close to the active area, stating that you should "Maintain a minimum die size in view of (a) the number of isolation regions, (b) the area of the isolation regions, (c) the area required for bonding pads, and (d) the area required for component interconnection", which clearly means keeping the die large enough to contain the isolation regions, bonding pads, and interconnect area separated from the die edge. That the meaning of "maintain" in this reference does not mean "minimize" as suggested by the Examiner, may be further seen in reference to summary point 4, using the term "Minimize" when referring to shrinking an area, and not "maintain a minimum", which is clearly against the teachings of the present application.

The cited '86 reference is used to show that semiconductor die are rectangular. Applicant submits that the reference discloses nothing suggesting reducing the size of the non active region of the die. The text indicated by the Examiner does not have any suggestion of flatter smoother scribe edges or reduced scribe line width.

Yamada is used to show that sawing scribe lanes using a diamond embedded resin saw blade is known in the art, and "results in a smooth, effectively polished surface", as stated on page 3 of the outstanding Office Action. Never-the-less, there is no disclosure that Applicant can find regarding the distance of the edge of the scribe lanes 2 from an edge of an active region, which is admitted by the Examiner on page 4, fourth paragraph of the outstanding Office Action. The importance of this dimension does not appear to be mentioned anywhere in the reference. The cited reference requires two cut operations, different width blades, different diamond mesh size, and different feed speeds, to form the scribe cut.

Altavela is used in the outstanding Office Action, but there is no discussion of the features contained in Altavela, either alone or in combination with the other references. The previous Office Action used Altavela to show a smooth surface lateral surface without polishing. Altavela discloses sawing the front surface of a thermal ink jet printer head so that the sawing leaves a front surface that does not require a polishing step (see Fig. 8 and col. 1, lines 7-14). Applicant submits that there is no suggestion of a scribe cut distance relative to the active circuitry area, which would be irrelevant for the described process.

The newly cited reference of Chittipeddi (U.S. 5,751,065) is used to show "that active circuitry is advantageously placed beneath a bond pad because this "is a more efficient use of silicon and there facilitates a larger number of dice per wafer"", which Applicant believes is incorrectly applied to the present application. The number of dice per wafer depends in part upon the length plus the width of the scribe lane in an X direction, multiplied by the width plus the width of the scribe lane in a Y direction of the die as imaged upon the wafer. This results in a die area, which determines the maximum number of dice on a wafer of a given area. The Chittipeddi reference is reducing the area of the die independent of the scribe area, which is not even shown or discussed in Chittipeddi. The suggestion on page 5 of the outstanding Office Action that it "would have been obvious to one of ordinary skill in the art at the time of the claimed invention to not only place metal features such as bond pads with 5 microns of the die

edge" appears to be incorrect since there is no discussion of scribe lines or die edges in the reference, and there is no suggestion of bringing the edge of a scribe lane closer to the edge of the die active region. This is not surprising, since bringing the edge of the scribe lane cut closer to the die active region does not have any impact on "a more efficient use of silicon and therefore facilitate a larger number of dice per wafer" (col. 2, lines 65-67). This is obvious to one of ordinary skill in the art since it is the original thickness of the scribe lanes as formed on the wafer prior to sawing or cutting that impacts the number of dice per wafer. Moving the scribe edge after sawing makes the individual die smaller, but does not impact the number of die per wafer.

Applicant submits that the statement on the bottom of page 4 of the outstanding Office Action that "Yamada and the other references admittedly do not disclose that "active circuitry" of the die is "within 5 microns of a side surface of the die" yet the combination of references "does show that a metal feature of active circuitry, such as a bond pad, is obviously as close to the die edge as possible", is incorrect, since there is no discussion of bringing scribe lane saw cut edges closer to the active region in any of the references, whether taken alone of in any combination. The references are concerned with reducing die size as imaged, which does impact total number of dice per wafer, while the present claims recite is that the edge of the inactive region is moved closer to the active edge after the die have been separated. This reduces the size of the package that the die may be fit into, a feature not discussed in any of the references, but does not have an impact on the number of dice per wafer.

Applicant respectfully submits that the suggested combination of references neither describes nor suggests at least the feature of "*...a substrate having a first planar surface having a first region with active circuitry including at least one of a transistor, resistor and a signal conductor thereon surrounded by an unused blank second region ... with a top portion of each individual planar perimeter side surface disposed in the second region and within 5 microns of an edge of active circuitry in the first region...*", as recited in independent claims 11 and 15, as amended herein. The cited references do not provide any disclosure or suggestion of a scribe edge within 5 microns of active devices as recited in claims 11 and 15, as amended herein.

The dependent claims are felt to be in patentable condition at least as depending from base claims shown above to be patentable over the references. In light of the above noted claim amendments, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Reservation of Rights

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney David Suhl at (508) 865-8211, or the undersigned attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 26 March '07 By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 26 day of March 2007.

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